23. The cache memory of claim 19, further comprising means for transforming a set index identifying a set in said cache memory for a block of main memory to an expanded group of sets including said thrashed set and one or more additional sets.

24. The cache memory of claim 19, wherein said means for identifying identifies said one or more additional frames to augment said thrashed set using an access rate of said additional frames.

25. The cache memory of claim 19, wherein said means for identifying identifies said one or more additional frames to augment said thrashed set using a position in an address space of said additional frames.

26. The cache memory of claim 19, further comprising means for disassociating said one or more additional sets from said thrashed set when the additional sets are no longer needed to decrease thrashing.

27. An integrated circuit, comprising:

a cache memory having a plurality of sets of cache frames for storing information from main memory;

a thrashing detector for determining when one or more of said sets are a thrashed set; and

a selector for identifying one or more additional frames to augment said thrashed set.

28. The integrated circuit of claim 27, wherein said thrashing detector evaluates a miss rate of a set.

29. The integrated circuit of claim 27, further comprising a mapper that transforms a set index identifying a set in said cache memory for a block of main memory to an expanded group of sets including said thrashed set and one or more additional sets.

30. The integrated circuit of claim 27, further comprising a mechanism for disassociating said one or more additional sets from said thrashed set when the additional sets are no longer needed to decrease thrashing.